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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/763,174	01/26/2004	Toru Tanzawa	248110US2S	6702
22850	7590	07/26/2005		
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C. 1940 DUKE STREET ALEXANDRIA, VA 22314			EXAMINER NGUYEN, HIEP	
			ART UNIT	PAPER NUMBER
			2816	

DATE MAILED: 07/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H.A

<b>Office Action Summary</b>	<b>Application No.</b> 10/763,174	<b>Applicant(s)</b> TANZAWA ET AL.	
	<b>Examiner</b> Hiep Nguyen	<b>Art Unit</b> 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
  - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 17 May 2005.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1,2 and 4-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☐ Claim(s) \_\_\_\_\_ is/are rejected.
- 7) ☒ Claim(s) 1,2 and 4-21 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01-26-04 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 6-8 and 13-15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and/or clarification is required.

Regarding claim 6, the recitation “wherein the comparison circuit includes as an output end, a connection node directly connecting between an output terminal of the first voltage/current conversion circuit and an output terminal of the second voltage/current conversion circuit” is indefinite because it is misdescriptive. The output of the comparison circuit (116) in figure 4 is the output of the comparison circuit which is not directly connecting between the output terminals of the first and second voltage/current conversion circuits. The same rationale is true for claim 13.

Regarding claim 7, the recitation “first current is a charging current which flows out from the output terminal, and the second current is a discharging current which flows into the output terminal” is indefinite because it is misdescriptive. The charging current should flow into the output terminal, and the second current is a discharging current which flows out from the output terminal”. The same rationale is true for claims 8, 14 and 15.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 6-10 and 13-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Gilbert (USP. 6,204,719).

Regarding claims 1 and 2, figure 4 of Gilbert shows a signal level detector comprising:

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a first voltage/current conversion circuit (13) which outputs a first current which depends on a voltage amplitude of an inputted signal ( $V_{in+}$ ,  $V_{in-}$ );

a second voltage/current conversion circuit (15) which outputs a second current which depends on an inputted reference voltage signal ( $V_{set+}$ ,  $V_{set-}$ ); and

a comparison circuit (18A) which compares the first current with the second current and outputs an output signal based on a comparison result,

wherein the first voltage/current conversion circuit outputs the first current which depends on a square of a voltage amplitude of the inputted signal, and the second voltage/current conversion circuit outputs the second current which depends on a square of an amplitude of the inputted reference voltage signal (col. 3, lines 30-57).

Regarding claim 6, the output of the comparison circuit (18A) is a node wherein the result of the comparison of the two input voltage is shown.

Regarding claims 7 and 8, figure 6 of Gilbert shows that the first current (flowing to node E1) is a charging current which flows out from the output terminal (E1), and the second current is a discharging current which flows into the output terminal. The flow of current could be reversed if the current flow is considered to be electron flow.

Regarding claims 9 and 10, figure 4 of Gilbert shows a signal level detector comprising:

a first squaring circuit (13) to which a first voltage signal ( $V_{in+}$ ,  $V_{in-}$ ) is inputted and which outputs a first current ( $I_1$ ) including a square component of an input amplitude of the first voltage signal;

a second squaring circuit (15) to which a reference voltage signal ( $V_{set+}$ ,  $V_{set-}$ ) is inputted and which outputs a second current ( $I_2$ ) including a square component of an amplitude of the reference voltage signal; and

a comparison circuit (18A) which compares a first output voltage which is in proportion to the first current with a second output voltage which is in proportion to the second current, and outputs a control signal ( $V_{out}$ ) used to detect the first voltage signal based on a comparison result.

Regarding claim 13, the output of the comparison circuit (18A) is a node wherein the result of the comparison of the two input voltages is shown.

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Regarding claims 14 and 15, figure 6 of Gilbert shows that the first current (flowing to node E1) is a charging current which flows out from the output terminal (E1), and the second current is a discharging current which flows into the output terminal. The flow of current could be reversed if the current flow is considered to be electron flow.

Regarding claims 16, 17, 18 and 19, figure 2 of Gilbert shows an amplification factor control system comprising:

- an amplification circuit (26) which output an output signal by amplifying a reception signal (RF) signal inputted thereto with an amplification factor according to a control signal, the output of the circuit (18) controls the gain of amplifier (26); and

- a signal level detector (12, 14, 16, 18) to which the output signal is inputted and which includes a first voltage/current conversion circuit (12) which outputs a first current (I1) which depends on a voltage amplitude of the output signal, a second voltage/current conversion circuit (14) which outputs a second current (I2) which depends on a reference voltage signal (Vset) inputted thereto, and a comparison circuit (16, 18) which compares the first current with the second current and outputs the control signal based on a comparison result.

The first and second currents have values depending upon the square of the voltage amplitude of the input signal.

Regarding claim 21, figure 4 of Gilbert shows a signal level detector comprising

- a first voltage/current conversion circuit (13) which outputs a first current which depends on a voltage amplitude of an inputted signal ( $V_{in+}$ ,  $V_{in-}$ ), the inputted signal being a differential signal;

- a second voltage/current conversion circuit (15) which outputs a second current which depends on an inputted reference voltage signal (Vset), the inputted reference voltage signal including two reference voltages; and

- a comparison circuit (18A) which compares the first current with the second current and outputs an output signal based on a comparison result.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 4, 5, 11, 12 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gilbert (USP. 6,204,719) in view of Kraz (US Pat. 6,563,319).

Regarding claims 4 and 5, figure 4 of Gilbert includes all the limitations of claims 4, 5, 11, 12 and 20 except for the limitation that there are capacitors and resistors coupled between the outputs of the first and second voltage/current conversion circuits and the ground. Figure 2 of Kraz shows a voltage/current conversion circuit having a capacitor (64) and a resistor (62) coupled between the output to the ground for charging and holding the output current of the voltage/current conversion circuit and for determining the decay of the output signal (col.5, lines 61-65; col. 6, lines 10-13). Therefore, it would have been obvious to one having skill in the art at the time the invention was made to implement the capacitors and the resistors taught by Kraz into the circuit of Gilbert between the outputs of the voltage/current conversion circuits and the ground for charging and holding the output current of the voltage/current conversion circuits and for determining the decay of the output signal.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen

07-22-05



**TUAN T. LAM**  
**PRIMARY EXAMINER**